

Digital Systems Design

Course Syllabus

Spring Semester 2005

EE/COSC 2390, MWF 10:00–10:50 AM, Room EN 3110

Abstract

This course will introduce the student to the fundamentals of digital systems, including number systems, combinational and sequential digital logic, state machines, and digital design. The use of professional-level EDA tools, including schematic capture, Verilog HDL, and design synthesis software is emphasized. Design approaches including SSI, MSI, and LSI gates along with CPLDs and FPGAs are covered.

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1 Instructor

Dr. Cameron H. G. Wright, P.E.

Office: EN 5052 *Phone:* 766-6104

E-mail: chgw@uwyo.edu

Web page: <http://wwweng.uwyo.edu/electrical/faculty/wright.html>

Office hours: (MW) 3:30–4:30 PM, (TT) 9:00–10:00 AM, or by appointment.

2 Course Goals and Objectives

Goal: The goal of this course is for the students to develop the ability to analyze an existing digital circuit or to synthesize a new digital design to meet stated specifications.

Objectives: Students will be able to

- Work with a variety of number systems and numeric representations, including signed and unsigned binary, hexadecimal, 2's complement.
- Apply fundamental analysis skills to correctly describe the behavior of a given digital logic circuit.
- Translate system requirements into a practical digital design, making use of modern EDA tools such as schematic capture, Verilog HDL, and logic synthesis programs.
- Demonstrate hands-on testbench skills and the ability to communicate appropriately via a lab notebook while functioning as part of an engineering lab team.

3 Course Prerequisites

The student must have satisfactorily completed MATH 2205 (*Calculus II*).

4 Course Grading

4.1 Breakdown of Graded Events

Graded material is given the following weights.

	Weight
Exam 1	20%
Exam 2	20%
Final Exam	25%
Homework	10%
Quizzes	10%
Laboratory	12%
Lab Notebooks (overall)	3%
Total	100%

Typically there will be one homework assignment and at least one quiz in class each week. Solutions to the homework will be posted on the course web site *after* the turn-in date. In most cases, just one problem from a given assignment will be graded; students are responsible for checking the web site to verify their solutions to the remaining problems. Exams will be given during normal class time.

Unless arranged for *ahead of time* by the student with the instructor, it is not possible to make up a missed quiz or exam without a University Excused Absence (available from the Office of Student Life). This policy is strictly observed.

4.2 Turn-In Policy

All homework assignments are due at the *beginning* of the lecture period (10:00 AM) on the associated due date (1 week from the assignment date unless otherwise stated). Students should use the unlined side of standard *engineering paper* to neatly record their homework solutions. The accepted turn-in method for the homework is to:

1. staple all sheets in the upper left corner,
2. fold all the sheets once (long-wise),
3. with the fold on the left, write your name and HW assignment number neatly at the top of the paper, and
4. place your homework on the table at the front of the classroom before lecture begins.

Hint: engineering problems are best solved using the “Given, Required, Solution, Answer” format. Be sure to write clearly and neatly. The Student Grader is *not* required to decipher inscrutable handwriting; you could end up with a zero if your homework is too difficult to read.

Late turn-ins will not be accepted unless an extraordinary situation exists. Very few circumstances constitute an extraordinary situation—plan ahead! You can always drop off your assignment at my office before the due date.

4.3 Grading Scale

The course will be graded on the following scale, where the student’s overall average in the course, as a percentage, is represented by x .

Grade	Average (%)
A	$90 \leq x \leq 100$
B	$80 \leq x < 90$
C	$70 \leq x < 80$
D	$60 \leq x < 70$
F	$0 \leq x < 60$

5 Course Materials and Resources

5.1 Textbook

The textbook used for EE/COSC 2390, by M. Morris Mano, is listed as [1] in the reference section of this syllabus. You will use this text extensively throughout the semester, as we will cover nearly the entire book. Take advantage of the many examples in the book and the selected answers to end-of-chapter problems in the appendix.¹

5.2 Web Site

For this section of EE/COSC 2390, I will make frequent use of the course web site at

<http://wwweng.uwyo.edu/classes/sp2005/ee2390/cwright/classinfo.html>.

A copy of this syllabus, assignments, homework solutions, and other supplemental material will be posted on this web site. You are responsible for checking it regularly.

5.3 Software and Other Resources

Each student must become familiar with the following software:

- Xilinx ISE 6.2i integrated programmable logic development environment, and
- Atmel WinCUPL Version 5.2 programmable logic compiler.

These tools are available in the ECE Digital Lab (EN 5030); the Xilinx tools are also available in the ECE Department Computer Lab (EN 5038).

See the reference section of this syllabus for an annotated bibliography of some helpful books. Be sure to regularly check the course web site for other information, including helpful web links and/or tutorials. I also plan to use your e-mail address throughout the semester, so be sure the correct address is listed on Hole-in-the-Wall.

6 Collaboration Policy

To solve the homework assignments and Prelabs, you are encouraged to work with other students currently enrolled in EE/COSC 2390. You must, however, document *any* of the help you receive in the form of comments directly on your homework paper or in your lab notebook as appropriate. No comments mean you are submitting the item as *totally* your own work; my assumption will always be that you are an honorable person unless you cause me to believe otherwise. Simply copying another person's assignment is not allowed—the actual item you turn in must ultimately be your own work and you may be called to my office to explain in detail the specifics of your work.

Quizzes and exams must always be the *student's own work* as noted in the Department of Electrical and Computer Engineering Course Policies (available in the Department Office) and the University of Wyoming Academic Policies and Procedures.

¹Chapter 10 of your text is an excellent reference for electrical and computer engineering students, who should take time to read this chapter on their own before the next semester. It will help with other classes. For computer scientists, Chapter 10 may be thought of as being in the “nice to know” category.

7 Laboratory

Important note: ***Attendance at labs is required.*** You must attend the lab section in which you are enrolled. Satisfactory completion of *each and every* lab exercise is *required* in order to pass the course. Refer to the EE/COSC 2390 Laboratory Policies handout for further details. *Note:* the first lab meeting will be on Monday, January 24, 2005.

The point above bears repeating, as someone in the class always has to find out the hard way: If you do not satisfactorily complete each and every lab exercise, you will fail the course, as specified in the policies and regulations of the Department of Electrical and Computer Engineering. That may sound harsh, but that's the deal.

8 Course Overview

Welcome to EE/COSC 2390! This course will prepare you to deal competently with myriad digital system design challenges that regularly confront electrical and computer engineers and computer scientists. The emphasis in EE/COSC 2390 is on fundamental principles and practical applications, rather than esoteric theory or arcane derivations.

Just like with anything worthwhile in life, if you aren't willing to put in the time and effort, you won't ever become good at it. Be prepared to devote considerable time and effort to this class. I promise to be sensitive to the time requirements of every assignment I give you, but *you* have to put forth the effort. As Robert E. Heinlein was known to say, "TANSTAF.".

Some recommendations for success in this class which you might want to consider...

Don't miss class. New material is covered each lecture. If you miss class, you are responsible for covering the missed material on your own. Repeat lectures will *not* be given during office hours.

Read in advance. The reading assignments are listed in the next section. Your textbook author has written many digital design and computer engineering texts, and your text in particular is considered one of the most "readable" in print. The argument "but the book is difficult to read" receives very little respect in any forum.

Start homework early. Give yourself some time to consider the problems and determine whether or not you need instructor assistance. Last-minute questions are a bad idea.

Don't ignore the homework, labs, and quizzes. They comprise 35% of your grade!

Ask questions. This includes during class, during discussions, and during office hours. I don't like a silent class—feel free to ask questions or make reasonable comments at will (but no distracting side conversations).

Don't arrive late for class. If you know you'll be delayed (or absent) for some reason, just let me know ahead of time in person or via e-mail. It's the courteous and adult thing to do.

Let's have fun in this class! I like lively, attentive, alert students with an active sense of humor. It's more fun that way for all of us...

9 Course Schedule

The following is an approximate lesson-by-lesson schedule, *subject to change*. Changes will be announced in class, sent via e-mail, or posted on the course web site.

	Date		Topic	Reading	Hwk Due
Jan	10	M	Intro, Number Systems, Complements	Ch. 1 pp. 1–13	
	12	W	Signed Addition/Subtraction, Overflow	Ch. 1 pp. 13–16	
	14	F	More Addition/Subtraction, Binary Codes	Ch. 1 pp. 16–24	
	19	W	Registers, Binary Logic	Ch. 1 pp. 24–30	
	21	F	Boolean Algebra and Functions	Ch. 2 pp. 33–44	Set #1 Due
	24	M	Canonical/Standard Forms, Other Logic	Ch. 2 pp. 44–53	
	26	W	Digital Logic Gates, Integrated Circuits	Ch. 2 pp. 53–61	
	28	F	Minimization of Gates, K-Maps	Ch. 3 pp. 64–79	Set #2 Due
Feb	31	M	Don't Cares, Implementations	Ch. 3 pp. 80–99	
	2	W	Finish Minimization, Intro to HDLs	Ch. 3 pp. 99–106	
	4	F	Combinational Logic Design	Ch. 4 pp. 111–128	Set #3 Due
	7	M	More Logic Design	Ch. 4 pp. 128–134	
	9	W	Decoders/Demultiplexers	Ch. 4 pp. 134–138	
	11	F	Encoders/Multiplexers	Ch. 4 pp. 139–147	Set #4 Due
	14	M	HDL for Combinational Logic Design	Ch. 4 pp. 147–154	
	16	W	More HDL, Test Benches	Ch. 4 pp. 155–160	
Mar	18	F	Review, with time for student questions	Notes, Ch. 1–4	Set #5 Due
	21	M	Exam #1	Ch. 1, 2, 3, 4	
	23	W	Synchronous Sequential Logic	Ch. 5 pp. 167–179	
	25	F	Analysis, State Diagrams	Ch. 5 pp. 180–190	
	28	M	HDL for Sequential Logic	Ch. 5 pp. 190–198	
	2	W	State Reduction and Assignment	Ch. 5 pp. 198–203	
	4	F	Design and Synthesis	Ch. 5 pp. 203–211	Set #6 Due
	7	M	More on Design and Synthesis	Ch. 5 pp. 203–211	
	9	W	Registers	Ch. 6 pp. 217–227	
	11	F	Counters	Ch. 6 pp. 227–239	Set #7 Due
	14–18	M–F	<i>Spring Break — No Classes</i>		
	21	M	More Counters	Ch. 6 pp. 239–244	
23	W	HDL for Registers and Counters	Ch. 6 pp. 244–249		
25	F	<i>Easter Break — No Classes</i>			
28	M	Memory, RAM	Ch. 7 pp. 255–267	Set #8 Due	
30	W	Error Detection and Correction, ROM	Ch. 7 pp. 267–276		
Apr	1	F	PLA, PAL, SPLD, CPLD, FPGA	Ch. 7 pp. 276–287	
	4	M	Review, with time for student questions	Notes, Ch. 5–7	Set #9 Due
	6	W	Exam #2	Ch. 5, 6, 7	
	8	F	Register Transfer Level (RTL)	Ch. 8 pp. 291–299	
May	11	M	Algorithmic State Machines (ASM)	Ch. 8 pp. 299–310	
	13	W	HDL Design Example	Ch. 8 pp. 310–317	
	15	F	More RTL, ASM, HDL	Ch. 8 pp. 291–317	Set #10 Due
	18	M	More Design Examples	Ch. 8 pp. 317–336	
	20	W	Intro to Asynchronous Sequential Logic	Ch. 9 pp. 342–349	
	22	F	Race conditions, stability	Ch. 9 pp. 349–352	Set #11 Due
	25	M	Debouncing switches	Ch. 9 pp. 359–360	
	27	W	Hazards	Ch. 9 pp. 379–384	
	29	F	Review, with time for student questions	Notes, Ch. 1–9	Set #12 Due
	2	M	Final Exam 10:15–12:15 am	Ch. 1–9	

References

- [1] M. M. Mano, *Digital Design*. Prentice Hall, 3rd ed., 2002. ANNOTATION: A very complete yet readable introductory text. Many excellent examples and the best treatment of Verilog HDL in a digital design text that I have ever seen.
- [2] C. Maxfield, *Bebop to the Boolean Boogie*. Newnes/Elsevier Science, 2nd ed., 2003. ANNOTATION: A truly great book! This book is fun to read; you can learn all about digital logic while being entertained by this talented author. Too bad it isn't quite suitable as a textbook, but you do get a good seafood gumbo recipe in the appendix!
- [3] J. F. Wakerly, *Digital Design: Principles and Practices*. Prentice Hall, 3rd ed., 2000. ANNOTATION: A densely written but extremely valuable book on digital design. Considered by many to be one of the best modern texts on the subject, it is sometimes used for introductory courses but mainly is used in more advanced courses. An excellent book for your professional library.
- [4] J. Bhasker, *A Verilog HDL Primer*. Star Galaxy Publishing, 2nd ed., 1999. ANNOTATION: A very easy to read introduction to Verilog, but a bit on the elementary side.
- [5] S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*. Prentice Hall PTR, 2nd ed., 2003. ANNOTATION: My favorite Verilog book. A bit harder to read than Bhasker, but very complete and well organized.
- [6] K. Coffman, *Real World FPGA Design with Verilog*. Prentice Hall PTR, 2000. ANNOTATION: A bit advanced, but as the title says it is full of real-world practical tips.
- [7] M. D. Ciletti, *Advanced Digital Design with the Verilog HDL*. Pearson/Prentice Hall, 2003. ANNOTATION: An advanced but very well written text with lots of examples.
- [8] M. D. Ercegovac and T. Lang, *Digital Arithmetic*. Morgan Kaufmann Publishers, 2004. ANNOTATION: A detailed treatment of all types of computer-based mathematics, number systems, and numerical representations.

Only one more page to go...

Finally...

Congratulations on reading this far! Lesser mortals gave up a page or two ago. As a reward, perhaps these quotes will inspire you in a positive manner...

*There comes a time in every man's life when he is called upon to do something very special for which he and he alone has the capabilities, has the skills, and has the necessary training. What a pity if the moment finds the man unprepared.*²

—WINSTON CHURCHILL

To study, and when the occasion arises to put what one has learned into practice—is that not deeply satisfying?

—CONFUCIUS

*They never said it would be easy, but they never said it'd be this hard.
They never said it would be easy, but I never thought we'd come this far.*

—SHERYL CROW

That which does not kill us makes us stronger.

—FRIEDRICH NIETZSCHE

²Here we interpret *man* to mean “a member of the human race.” This quote fully applies to both men and women, and no gender bias is intended.